37

Notice of Allowability	Application No.	Applicant(s)	
	10/519,799	SAKAI ET AL.	
	Examiner	Art Unit	
	Victor V. Yevsikov	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *paper, filed 09/25/2006*.

2. ☒ The allowed claim(s) is/are *1-7,10-15 and 25-28*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 12/29/04
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Allowable Subject Matter

Claims 1-7, 10-15 and 25-28 are allowed.

The following is an examiner's statement of reasons for allowance:

Regarding claims 1-7, 25 and 27, prior art does not teach a method of producing a semiconductor integrated circuit device, comprising the steps of:

(a) forming a high dielectric constant insulating film over a semiconductor substrate;

(b) forming a conductive film over the high dielectric constant insulating film;

(c) forming a mask film over the conductive film;

(d) selectively removing the mask film thereby forming a mask pattern;

(e) etching the conductive film by using the mask film having the mask pattern as a mask thereby forming a conductor piece;

(f) removing the mask film in a state of leaving the high dielectric constant insulating film on both ends of the conductor piece over the semiconductor substrate; and

(g) after the step (f), removing the high dielectric constant insulating film on both ends of the conductor piece over the semiconductor substrate;

(h) after the step (q), forming semiconductor regions in the semiconductor substrate; and

(i) after the step (h), forming sidewall on side surfaces of the conductor piece by depositing an insulating film and anisotropically etching the insulating film.

Regarding claims 10-15, 26 and 28, prior art does not teach a method of producing a semiconductor integrated circuit device, comprising the steps of:

(a) providing a semiconductor substrate with a first insulating film formed over a first region of the semiconductor substrate and a second insulating film formed over a second region of the semiconductor substrate;

wherein a thickness of the first insulating film is greater than a thickness of the second insulating film;

(b) forming a high dielectric constant insulating film over the first insulating film and over the second insulating film;

(c) forming a conductive film over the high dielectric constant insulating film;

(d) forming a mask film over the conductive film;

(e) selectively removing the mask film thereby forming a mask

(f) etching the conductive film by using the mask film having the mask pattern as a mask thereby forming conductor pieces over the first regions and over the second regions;

(g) removing the mask film in a state of leaving the high dielectric constant insulating film on both ends of the conductor piece over the first region and over the second region;

(h) after the step (g), removing the high dielectric constant insulating film on both ends of the conductor pieces over the first region and over the second region;

(i) after the step (h), forming first semiconductor regions in the first region and forming second semiconductor regions in the second region; and

(j) after the step (i), forming sidewalls on side surfaces of the conductor pieces by depositing an insulating film and anisotropically etching the insulating film.

Ota (US 2002/0047170), Maeda (US 2002/0052086) and Yamazaki (US 2001/0028093) teach methods to provide a high dielectric constant insulating film over a semiconductor substrate and forming sidewall on side surfaces of the conductor piece by depositing an insulating film.

However, prior art does not teach methods wherein removing the mask film in a state of leaving the high dielectric constant insulating film on both ends of the conductor piece over the semiconductor substrate; removing the high dielectric constant insulating film on both ends of the conductor piece over the semiconductor substrate; forming semiconductor regions in the semiconductor substrate; and forming sidewall on side surfaces of the conductor piece by depositing an insulating film and anisotropically etching the insulating film.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Ota (US 2002/0047170), Maeda (US 2002/0052086) and Yamazaki (US 2001/0028093) teach method to provide a high dielectric constant

insulating film over a semiconductor substrate and forming sidewall on side surfaces of the conductor piece by depositing an insulating film.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor Yevsikov whose telephone number is (571) 272-1910. The examiner can normally be reached on Monday –Thursdays 8:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, examiner's supervisor, William B. Baumeister, can be reached on (571) 272-1722. The fax phone numbers for the organization where this application or processing is assigned is (703) 873-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published application may be obtained from either Private PAIR or Public PAIR. Status information for unpublished application is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

V. Yevsikov

Victor Yevsikov
Examiner
Art Unit 2891

October 12, 2006

Asok Kumar Sarkar
10/12/06

ASOK K. SARKAR
PRIMARY EXAMINER